ECE 522-301

Summer 2014 intersession (May 15, 2014 – June 14, 2014)

MWTR 8.00-10.20am, ENGR A420

Instructor: Spyros Tragoudas, email: spyros@siu.edu, phone: 618 453 7027, office hours: MTWR 10.20-noon or by appointment

GA: Wisam AlJubouri, wisam@siu.edu, 618 453 7659, Lab hours: TBD

Textbook:

(b) Papers published in journals and conference proceedings
(c) Notes

Topics:

(a) Fault modeling
(b) Structural (logical faults) and the single stuck-at model: Fault simulation, Test pattern Generation, compaction in combinational and sequential logic, design for testability
(c) Delay faults (path delay and transition faults): Fault simulation, Test pattern Generation, compaction in combinational and sequential logic, design for testability
(d) Memory fault modeling and march tests
(e) IQQD (time-permitting)

Workload:
2 exams (mid-term and final exam), 30% each
Lab assignments: total 10%
Projects: total 30%