ECE 520 Syllabus
Fall 2015

Instructor: Prof. Spyros Tragoudas
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Office Hours: Tuesday & Thursday, 11:00am - 2:00pm or by appointment
Lecture: T&TR 8.00-9.15am, EGR A-222

Teaching Assistant (TA): Pavan Javvaji, pavan.javvaji@siu.edu
Lab hours & TA hours: Tuesday 5:00-6:15pm ENGRE-132 (Sun workstation Lab) or ENGRA-220
Thursday 5:00-6:15pm ENGRE-132 (Sun workstation Lab).
(occasionally) Friday 8-8:50am ENGRE-132 or ENGRA-320

Grading/Evaluation:
- Three exams: Each 18% of the total grade.
- Laboratory assignments: 36% of the total grade
- 2 projects: with a total of 10% of the grade

A: 90-100; B: 80-89; C: 70-79; D: 60-69; F: 0-59

Classroom Policies:
A. Students are responsible for all announcements made in class and/or posted to D2L.
B. Late Laboratory assignments are not accepted.
C. No make-up exams.
D. Third exam will be given on the finals week.
E. Cell phone usage is not allowed during lecture.

1. Course number and name: ECE 520 VLSI Design and Test.
2. Credits and contact hours: 3 credits, Two 75-minute sessions per week, Two 75-minute sessions per week in the Unix lab.
   The course material will be supplemented using notes that will be given in class.
   Other supplementary textbooks:
5. Specific course information
   a. The course covers all the phases of Electronic Design Automation. Laboratory experiments on existing tools will supplement the lectures. Projects will supplement the laboratory assignments.
   b. Prerequisites: Equivalents of ECE 329, ECE 345 or consent of instructor
6. Instructional Objectives
The student is expected to have a clear understanding of:

1. VHDL principles for VLSI CAD.
2. Algorithmic and graph theoretic concepts necessary for design automation.
3. Principles of CMOS VLSI design.
4. During the lab sessions they will become familiar with the VHDL simulator of the Cadence (or equivalent) design automation tools.
5. In addition, through a programming project in C, such as a three valued algebra combinational circuit simulator at the logic level, they will gain programming skills for VLSI CAD.
6. Techniques for automated synthesis and verification of digital combinational and sequential systems.
7. Techniques for tool development in timing analysis, testing, and concepts in high level synthesis.
8. During the lab sessions they will become familiar with the:
   i) Ambit tools (for synthesis).
   ii) SIS package (for synthesis).
   iii) Atalanta tools of Cadence (for testing).
   iv) Equivalent design automation tools for the above design automation areas.
   v) In addition they will gain experience in programming using existing tools in VLSI CAD. This will be accomplished through a more advanced programming project such as a program for logic or timing verification that is built on top of existing packages.
10. Methods for physical design automation.
11. During the lab sessions they will become familiar with Cadence physical design automation tools with installed libraries to experiment with the generation of automated layouts in sub micron technology that meet certain specifications associated to area, performance, crosstalk, power consumption and SIS tools will also be used for technology mapping.

7. **Brief list of topics (class, lab and project) to be covered**

a. **Classroom Topics**
   - Principles of CMOS technology. (Approximately 2 classes)
   - Graphs and graph algorithms. (Approximately 3 classes)
   - An overview of VHDL. (at the lab sessions)
   - Logic Synthesis.(Approximately 4 classes)
   - System and High Level Synthesis. (Approximately 4 classes)
   - Simulation. (Approximately 2 classes)
   - Fault modeling and design for testability. (Approximately 3 classes)
   - Fault simulation Automatic Test Pattern Generation.(Approximately 3 classes)
   - Timing analysis. (Approximately 2 classes)
   - Floorplanning. (Approximately 2 classes)
   - Placement and Partition. (Approximately 2 classes)
   - Routing. (Approximately 1 class)

b. **Laboratory Topics**
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• Introduction to Unix, cadence and synopsys tools. (2% - 3 sessions)
• Logic Simulation. (5% - 3 sessions)
• Testbench on Datapath Portion. (3% - 4 sessions)
• High Level Synthesis. (5% - 4 sessions)
• Logic Synthesis for Area and Delay Optimization. (6 % - 4 sessions)
• Static Timing analysis. (5%- 4 sessions)
• Testing. (4% - 3sessions)
• Physical Design - Floorplanning, Placement & Routing. (6%- 3 sessions)

c. Projects
• Logic and Fault Simulation Project 1. (5% approximately 6 sessions)
• Logic and Fault Simulation Project 2. (5% approximately 6 sessions)

8. CAD and Computer Tools Used: Cadence, Synopsys, Binary Decision Diagrams.