ECE–521 Fault–Tolerant Computer Design

FALL 2013
MW 8:35–9:50am, ENGR-D-131

DESCRIPTION: Fault–Tolerance; Hardware, software, information and time redundancy techniques; Error Correcting Codes; Design for Testability; Fault Models; Fault Simulation; Test Pattern Generation; Test Response Analysis; Built–In Self–Test; Scan techniques for sequential circuits.

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Office hours: Tue.Thu.: 9:00–12:00

TEACHING ASSISTANT: TBA

M. Abramovici, M. Breuer, A. Friedman, IEEE Press.
Notes/Handouts: given out in class.

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COURSE OUTLINE

Fault–Tolerance as a design objective.
Redundancy for fault–tolerance.
Error–Correcting Codes.
Fault models and relations. Fault Simulation.
Automatic Test Pattern Generation.
Built–In Self–Test. Mechanisms for test pattern application and verification.
Design for Testability. Scan designs.